10. (New) The semiconductor device of claim 9 wherein said ratio is about 0.2.

11. (New) The semiconductor device of claim 4 wherein said second silicon epitaxial layer has a thickness of about 100 nanometers.

12. (New) The semiconductor device of claim 11 wherein said cap layer has a thick of about 100 nanometers.

ABSTRACT OF THE DISCLOSURE

Please substitute the attached abstract for the current abstract.

REMARKS

Claims 1-2 were pending and under consideration, claim 3 having been withdrawn from consideration pursuant to an election.

In the Office Action of February 20, 2002, claims 1 and 2 were rejected and an objection was raised with respect to the abstract. Claim 1 was rejected as being anticipated by *Kubo et al.* Claim 2 was rejected as obvious in view of *Imai et al* and *Chu et al.* The abstract was deemed too long.

In response, Claim 1 has been re-written as new claim 4, and several new dependent claims added. The abstract has also been re-written.

With respect to the reject of claim 1, claim 5 recites a specific series of layers formed on each other, as opposed to over each other. Claim 5 also recites that the source/drain regions of the n-channel device are provided within the second silicon epitaxial layer formed on the first silicon layer and the first silicon layer formed on said relax layer, while the source/drain regions of the p-channel device are provided within the silicon-germanium compound layer formed on the substrate and the silicon cap layer formed on the silicon-germanium compound layer.

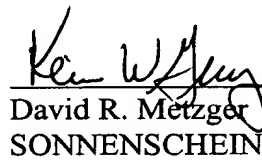
Kubo et al fails to fairly teach or suggest this structure. In contrast, it is clear that the source/drain regions are not so confined, nor are the silicon-germanium layers

so bounded. Accordingly, *Kubo et al* does not anticipate claim 4, nor any of the dependent claim 5-12.

With respect to the rejection of claim 2, the subject matter of claim 2 has been incorporated in to claim 4, and thus the rejection is moot. In any event, neither *Imai et al* nor *Chu et al.*, nor the combination of them fairly teaches or suggests a device having the layers as recited and the source/drain regions so confined.

Accordingly, it is submitted that claims 4-12 are patentable and that the application is in condition for allowance. Notice to that effect is requested.

Respectfully submitted,



(Reg. No. 32,919)

David R. Metzger
SONNENSCHEIN NATH & ROSENTHAL
P. O. Box 061080
Wacker Drive Station - Sears Tower
Chicago, Illinois 60606-1080
Telephone (312) 876 8000
Customer #26263

MARKED-UP VERSION WITH CHANGES MADE

IN THE CLAIMS

Please cancel claims 1-3 and add claim 4-12 as follows:

4. (New) A semiconductor device with p-channel and n-channel field effect devices formed on a common substrate, comprising:

a silicon substrate with p-channel and n-channel field effect regions corresponding to said p-channel and n-channel field effect devices, respectively,

said n-channel field effect region having a silicon-germanium buffer layer on said substrate, a silicon-germanium compound relax layer on said buffer layer, a first silicon layer formed on said relax layer and a second silicon epitaxial layer formed on said first silicon layer,

a concentration of germanium in said buffer layer being graduated so that it increases proceeding from a substrate side of said buffer layer to a relax layer side of said buffer layer, a concentration of germanium in said relax layer being substantially the same as the concentration of germanium at said relax layer side of said buffer layer,

said p-channel field effect region having a silicon-germanium compound layer formed on said substrate and a silicon cap layer formed on said silicon-germanium compound layer,

drain and source regions of said n-channel field effect device being within said second silicon epitaxial layer formed on said first silicon layer and said first silicon layer on said relax layer, and

drain and source regions of said p-channel field effect device being within said silicon-germanium compound layer formed on said substrate and said silicon cap layer formed on said silicon-germanium compound layer.

5. (New) The semiconductor device of claim 4 wherein, a ratio of germanium to silicon in said buffer layer increase from 0.0 to less than about 0.5 proceeding from said substrate side to said relax layer side of said buffer layer.

6. (New) The semiconductor device of claim 5 wherein, the ratio of germanium to silicon in said buffer layer is not greater than about 0.3.

7. (New) The semiconductor device of claim 4 wherein said buffer layer is about 1.68 micrometers thick and said relax layer is about 0.6 micrometers thick.

8. (New) The semiconductor device of claim 7 wherein said silicon-germanium compound layer in said p-channel field effect region has a thickness of about 100 nanometers.

9. (New) The semiconductor device of claim 4 wherein said silicon-germanium compound layer has a ratio of germanium to silicon of about 0.1 to less than about 0.8.

10. (New) The semiconductor device of claim 9 wherein said ratio is about 0.2.

11. (New) The semiconductor device of claim 4 wherein said second silicon epitaxial layer has a thickness of about 100 nanomaters.

12. (New) The semiconductor device of claim 11 wherein said cap layer has a thick of about 100 nanometers.